International Journal of Electrical and Electronics Engineering Research (IJEEER)
ISSN(P): 2250-155X; ISSN(E): 2278-943X
Vol. 4, Issue 2, Apr 2014, 83-90

TRANS STELLAR
• Journal Publications • Research Consultancy

DESIGN OF A 4-BIT VEDIC MULTIPLIER USING TRANSISTORS

RAMYA K. V & SUNIL KUMAR S. MANVI

Department of ECE, Reva Institute of Technology Bangalore, Karnataka, India

ABSTRACT

CMOS Logical circuits are widely used in the designing of Power and area efficient multiplier in various digital signal processors. The ancient philosophy of Vedic multiplication advantage can be taken for the multiplier implementation with the help of "Urdhva Tiryak Bhyam sutra". In almost all the processors, multiplier p lays a vital role & contributes substantially to the total power consumption of the system. This is very reliable because of the use of the Vedic algorithm (sutras) that reduces the number of computational steps to a great extent compared to any conventional method. This paper presents a high performance multiplier which has the maximum power reduction compared to gate level analysis. The schematic for this multiplier is designed using CADENCE tool. The design is then simulated in ADE using spectra in 180nm CMOS technology library file.

KEYWORDS: Component, Multiplier,Vedicalgorithms, Urdhva Tiryak Bhyam Sutra